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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,846	08/22/2003	Se Jun Heo	1670.1013	8145

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EXAMINER	
SANTIAGO, MARICELI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,846	HEO ET AL.	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-17 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-17 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Amendment, filed on February 28, 2006, has been entered and acknowledged by the Examiner.

Cancellation of claims 2, 3 and 18 has been entered.

Claims 1, 4-17 and 19-25 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 7, 8, 10, 11, 17, 19, 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Codama et al. (US 6,307,3 17).

Regarding claims 1, 17 and 22, Codama discloses an EL device and a method of making the same, comprising a substrate (1), a first electrode unit comprising first electrodes (5) formed on the substrate, first electrode terminals (not shown but required to drive the display, Column 1, lines 39-43) connected to the respective first electrodes, a second electrode unit comprising second electrodes (4) formed over the first electrodes (see Figs. 2 and 3), and second electrode terminals (2, 3) connected to the respective second electrodes, an emission area formed where the first electrodes intersect the second electrode, an EL layer (7) disposed between the first electrodes and the second electrodes in the emission area, an inter insulating layer (6, layer contacting left side of electrode 5 in Fig. 3) provided under the EL layer and covering a space between each of the plurality of lines of the first electrodes and an edge

portion of a top surface of each of the plurality of lines of the first electrodes, and an outer insulating layer (6, layer contacting right side of electrode 5 in Fig. 3) between the emission area and the second electrode terminals, wherein the outer insulating layer comprises an insulating material formed to contact at least an edge of the second electrode terminals facing the emission area to reduced a steepness of a step between the second electrode terminals and the substrate (Fig. 3).

Codama fails to explicitly exemplify the limitation of the first electrodes formed as a plurality of parallel evenly spaced lines and the second electrodes extending in an orthogonal direction with respect to the first electrodes. However, in the same field of endeavor, Miyaguchi discloses an EL device further comprising a first electrode unit comprising first electrodes (R1) formed as a plurality of parallel evenly spaced lines on the substrate, and a second electrode unit comprising second electrodes (L1) formed in an orthogonal direction with respect to the first electrodes over the first electrodes (Column 2, lines 49-62). At the time the invention was made, it would have been an obvious matter of design engineering to a person of ordinary skill in the art to provide the first electrodes as a plurality of parallel evenly spaced lines and second electrodes formed in an orthogonal direction with respect to the first electrodes as disclosed by Miyaguchi since applicant's claimed first and second electrodes configuration does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teaching applied. Furthermore, one skilled in the art would reasonable expect applicant's invention to perform equally well with either the electrode configuration disclosed by Codama or the electrode configuration disclosed by Miyaguchi since both arrangements perform the same function of providing the light emitting regions or pixel unit at the intersection the first and second electrodes. Accordingly, it would have been an obvious matter of design engineering to

modify the device of Codama in view of Miyaguchi to obtain the invention as specified in claim 1.

Regarding claim 4, Codama discloses the substrate comprising glass or plastic (Column 8, lines 29-35).

Regarding claims 7, 8, 19, 20 and 23, Codama discloses the outer insulating layer covering at least an edge (right edge) of the first electrode closest to the second electrode terminal covered by the outer insulating layer and the edge of each of the second electrode terminals facing the emission area (Fig. 3).

Regarding claims 10 and 11, Codama discloses the second electrode passing over the outer insulating layer to contact the second electrode terminals (Fig. 3).

Claims 1, 4-8, 10-14, 17, 19-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyaguchi et al. (US 6,297,589) in view of Tadokoro et al. (EP 1 022 931).

Regarding claims 1, 17 and 22, Miyaguchi discloses an EL device and a method of making the same, comprising a substrate (1), a first electrode unit comprising first electrodes (R1, G1, B1) formed on the substrate as a plurality of parallel evenly spaced lines (Fig. 1), and first electrode terminals (T, Fig. 4) connected to the respective first electrodes, a second electrode unit comprising second electrodes (L1, L2) formed in an orthogonal direction with respect to the first electrodes over the first electrodes (Figs. 1 and 2A), an emission area formed where the first electrodes intersect the second electrodes, an EL layer (4) disposed between the first electrodes and the second electrodes in the emission area, an inter insulating layer (2, Fig. 2A) provided under the EL layer and covering a space between each of the plurality of lines of the first electrodes and an edge portion of a top surface of each of the plurality of lines of the first electrodes, and an outer insulating layer (2, portion of layer in the periphery, outside

emission area). Miyaguchi is silent regarding the limitation of the second electrode unit comprising second electrode terminals, wherein the outer insulating layer is formed to contact at least an edge of the second electrode terminal facing the emission area.

However, in the same field of endeavor, Tadokoro discloses an EL device having a second electrode unit comprising second electrodes and second electrode terminals, wherein an outer insulating layer is formed to contact at least an edge of the second electrode terminal facing the emission area with the purpose of improving the contrast and the esthetics of the device by avoiding portions of the display to exhibit different colors due to the different components (Column 4, lines 10-23, and Column 9, lines 18-32). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide second electrode terminals with an outer insulating layer being formed to contact at least an edge thereof in order to improve the contrast of the device. Accordingly, the exhibition of different colors caused by the different components of the display (electrodes, terminals, uncovered parts of the substrate) is reduced, which is favorable from an esthetical point of view.

Regarding claim 4, Miyaguchi discloses the substrate comprising glass (Column 3, lines 46-47).

Regarding claim 5, Miyaguchi-Tadokoro discloses the second electrode terminals comprising a first terminal portion made of ITO and a second terminal portion comprising Cr (see EP '931, paragraph [0031]).

Regarding claim 6, Miyaguchi discloses the first electrode terminals being integrally formed with the first electrodes (Figs. 3-4).

Regarding claims 7-8, Miyaguchi-Tadokoro discloses the outer insulating layer covering at least an edge of the first electrode closest to the second electrode terminal covered by the

outer insulating layer and the edge of each of the second electrode terminals facing the emission area (Figs. 1 and 2A of '589, in view of Fig. 6 of EP '931).

Regarding claims 10-11, Miyaguchi-Tadokoro discloses the second electrode passing over the outer insulating layer to contact the second electrode terminals (Figs. 1 and 2A of '589, in view of Fig. 6 of EP '931).

Regarding claims 12-14, 21 and 25, Miyaguchi-Tadokoro discloses the claimed invention except for the limitation of forming a first buffer layer insulated from the first electrodes and the second electrode terminals. Miyaguchi-Tadokoro discloses a dielectric layer reducing a steepness of a step between the second electrode terminals and the substrate (Figs, 1 and 2A of '589, in view of Fig. 6 of EP '931).

However, Tadokoro discloses a method of forming an EL layer wherein the substrate is coated with a conductive layer comprising ITO, said layer being patterned into first electrodes, first electrode terminals and second electrode terminals. Tadokoro further discloses to apply a dielectric layer to insulate the respective patterns. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to leave an insulated pattern of the ITO layer between the first electrodes and the second electrode terminals in order to reduce the amount of material that is wasted in the manufacture of the device, and reducing the amount of dielectric material which is needed to accomplish the steepness reduction step of Tadokoro, resulting in a manufacture cost reduction of the device.

Regarding claims 19, 20 and 23, the claims are rejected over the reasons stated in the rejection of claims 7 and 8.

Claims 9, 15, 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyaguchi et al. (US 6,297,589) in view of Tadokoro et al. (EP 1 022 931), and further in view of Okuyama et al. (US 6,531,815).

Regarding to claims 9 and 24, Miyaguchi-Tadokoro discloses the claimed invention except for the limitation of via holes formed at portions of the insulating layer covering the edge of the second electrode terminal.

However, in the same field of endeavor, Okuyama discloses an EL device (Figs. 38 and 6B) including an insulating layer (PLN2) comprising via holes so electrodes are connected to a terminal through said via holes, and teaches this embodiment to provide a connection having a substantially wide width, which lowers the resistance (Column 9, lines 35-36). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form via holes at portions of the insulating layer in order to provide a connection having a substantially wide width, which lowers the resistance. Further, it has been held to be within the level of ordinary skill in the art to vary the shape of a component, i.e. forming via holes.

Regarding claims 15 and 16, Miyaguchi-Tadokoro discloses the claimed invention except for the limitation of a second buffer layer provided over a top surface of the substrate.

However, in the same field of endeavor, Okuyama discloses an EL device comprising a buffer layer including SiO_2 disposed over a top surface of a substrate with the purpose of acting as a stopper against impurities eluted from the glass substrate (Column 12, lines 1-5). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a buffer layer over the substrate, in order to prevent impurities from the substrate to reach the EL element.

Response to Arguments

Applicant's arguments filed February 28, 2006, in regards to the rejection of claims 1, 4-8, 10-17 and 19-25 over Miyaguchi et al. (US 6,297,589) in view of Tadokoro et al. (EP 1 022 931), or over Miyaguchi-Tadokoro in view of Okuyama et al. (US 6,531,815), have been fully considered but they are not persuasive.

Applicant contention that the applied prior art of reference (Miyaguchi '589, Tadokoro '931 or of Okuyama '815) fail to teach or suggest the "outer insulating layer between the emission area and the second electrode terminals ... to contact at least an edge of the second electrode terminals facing the emission area to reduce a steepness of a step between the second electrode terminal and the substrate" as expressly defined in Applicants, since the insulating layer in the applied references is deposited to cover the whole surface of the transparent electrode layer except for locations where display electrodes and terminals are present, is not found persuasive. The reference to Miyaguchi discloses an intermediate insulating layer having a inter section located between and separating the plurality of parallel spaced apart electrode lines, and further discloses an outer section of the insulating layer located at an outside peripheral area where the electrode terminals would be located. Although Miyaguchi is silent in regards to the second electrode unit comprising second electrode terminals, and the outer insulating layer being formed to contact at least an edge of the second electrode terminal facing the emission area, the teachings stated in the reference to Tadokoro provide for the missing limitations. Applicant's claimed invention does not exclude for the inter and outer insulating layers to be manufactured from a single insulating layer, as long as an inter section provided under the electroluminescent layer and covering a space between each of the plurality of lines of the first electrodes and an edge portion of a top surface of each of the plurality of lines of the first electrodes is provided between the parallel electrodes, and an outer

section formed to contact at least an edge of the second electrode terminals facing the emission area to reduce a steepness of a step between the second electrode terminal and the substrate is provided. Accordingly, it is the examiner's position that the claimed limitations are disclosed by the combination of Miyaguchi et al. (US 6,297,589) in view of Tadokoro et al. (EP 1 022 931).

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. However, applicant's amendment, filed September 8, 2005, necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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